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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/510,679	10/08/2004	Yoshinori Miyaki	XA-10186	4946

181 7590 12/21/2005

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
KUNZER, BRIAN	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/510,679	MIYAKI ET AL.	
	Examiner	Art Unit	
	Brian Kunzer	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 22 November 2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 39-57 is/are pending in the application.

4a) Of the above claim(s) 39-46 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 47-57 is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/343,701.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/8/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 47-57 in the reply filed on November 22, 2005 is acknowledged.

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "Manufacturing Method of a Semiconductor Device Utilizing a Flexible Adhesive Tape."

2. The disclosure is objected to because of the following informalities: In paragraphs [0208] and [0209] applicant states:

> "an insulating adhesive which is stronger in its adhesion to an adhesive (first adhesive) 26 for bonding a tape 1a and copper foil than in its adhesion to the silicon substrate of the semiconductor element 4"

Note that this is counter-intuitive to what is shown in fig. 39D and the direct opposite of what is claimed in claim 47. Examiner believes this is either a typing or translation error. Appropriate correction is required.

Claim Objections

Claim 52 is objected to because of the following informalities: Claim 52 recites the exact same limitation as claim 51. Examiner believes claim 52 is a result of a typing error and therefore will not be examined on any other merits than those pertaining to the examination of claim 51. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 49, 53, 55, 56 are rejected under 35 U.S.C. 102(b) as being anticipated by Li (US Patent No. 6,348,729).

With respect to claim 49, Li teaches, from figs. 6-10 and columns 3 and 4, a method of manufacturing a semiconductor device, comprising the steps of:

providing a flexible tape (250) having a plurality of terminals (222a, 224) in a product forming portion formed over a main surface of the tape, the terminals being formed by a metal film (see column 3, lines 16-26); (fig.6)

fixing a semiconductor element (210) to the main surface of the tape (250); (fig. 7)

connecting electrodes formed over the semiconductor element (210) and the terminals (222a, 224) with each other through conductive wires (230, 232); (fig. 8)

forming an insulating resin layer (240) in an area including the semiconductor element (210) and the wires (230, 232) over the main surface of the tape (250) to cover the semiconductor element (210) and the wires (230, 232); (fig. 9) and

peeling the tape (250) from the insulating resin layer (240) after covering the semiconductor element (210) and the wires (230, 232) with the insulating resin layer (240),

wherein the product forming portion comprises a semiconductor element fixing tape surface (area under 210) for fixing the semiconductor element (210) and a plurality of terminals (22a and 224) arranged around the semiconductor element fixing tape surface (area under 210).

With respect to claim 53, Li teaches, from figs. 6-10 and columns 3 and 4, a method of manufacturing a semiconductor device, comprising the steps of:

providing a flexible tape (250) having a plurality of terminals (222a, 224) in a product forming portion formed over a main surface of the tape, the terminals being formed by a metal film (see column 3, lines 16-26); (fig.6)

fixing a semiconductor element (210) to the main surface of the tape (250); (fig. 7)

connecting electrodes formed over the semiconductor element (210) and the terminals (222a, 224) with each other through conductive wires (230, 232); (fig. 8)

forming an insulating resin layer (240) in an area including the semiconductor element (210) and the wires (230, 232) over the main surface of the tape (250) to cover the semiconductor element (210) and the wires (230, 232); (fig. 9) and

peeling the tape (250) from the insulating resin layer (240) after covering the semiconductor element (210) and the wires (230, 232) with the insulating resin layer (240),

wherein the terminals (222a, 224) each inherently comprise a main metal layer (222a, 224) and one or plural auxiliary metal layers (not shown in figure, see column 3, lines 16-26) formed over a main surface of the main metal layer or over both the main surface and a back surface of the main metal layer.

With respect to claim 55, Li teaches, from column 3, lines 16-26, the auxiliary metal layer (gold plating) over the main surface of each of the terminals (222a, 224) is formed by a gold layer (gold plating).

With respect to claim 56, Li teaches that the lead frame (220), encompassing terminals (222, 222a, and 224) have a main metal layer made of copper. (See column 3, lines 39-50)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US Patent No. 6,348,729) in view of Nakazawa (US Patent No. 6,429,043).

With respect to claim 47, Li teaches, from figs. 6-10 and columns 3 and 4, a method of manufacturing a semiconductor device, comprising the steps of:

providing a flexible tape (250) having a plurality of terminals (222a, 224) in a product forming portion formed over a main surface of the tape, the terminals being formed by a metal film (see column 3, lines 16-26); (fig.6)

fixing a semiconductor element (210) to the main surface of the tape (250); (fig. 7)

connecting electrodes formed over the semiconductor element (210) and the terminals (222a, 224) with each other through conductive wires (230, 232); (fig. 8)

forming an insulating resin layer (240) in an area including the semiconductor element (210) and the wires (230, 232) over the main surface of the tape (250) to cover the semiconductor element (210) and the wires (230, 232); (fig. 9) and

peeling the tape (250) from the insulating resin layer (240) after covering the semiconductor element (210) and the wires (230, 232) with the insulating resin layer (240).

Li does not teach that the semiconductor element is bonded to the tape through an insulating adhesive which is stronger in its adhesion to the semiconductor element than in its adhesion to the tape, and in the step of peeling the tape from the insulating resin layer, the tape is peeled while allowing the adhesive to remain over a back surface of the semiconductor element.

However, Nakazawa, drawn to the manufacture of semiconductor packages, teaches, from figs. 5A-5E, the semiconductor element (11) is bonded to the tape (21) through an insulating adhesive (16) which is stronger in its adhesion to the semiconductor element (11) than in its adhesion to the tape (21), and in the step of peeling the tape from the insulating resin layer (17), the tape is peeled while allowing the adhesive (16) to remain over a back surface of the semiconductor element (11). (See process 4 which begins on column 7, line 65.)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the method of chip manufacturing of Li utilizing an insulating adhesive - as described by Nakazawa – because this prevents any unwanted electrical connections being made between the semiconductor element and any conductive paths beneath the semiconductor chip.

5. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US Patent No. 6,348,729) and Nakazawa (US Patent No. 6,429,043) as applied to claim 47 above, and further in view of Corisis (US Patent No. 6,903,464).

Li and Nakazawa teach the manufacturing method as detailed above.

Li and Nakazawa do not specifically teach that the adhesive is an adhesive tape.

However, Corisis, drawn to semiconductor die packages, teaches from fig. 5 and column 4, lines 31-54, a semiconductor element (12) fixed to a surface (14) through the use of an adhesive tape (27).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the method of manufacture of Li and Nakazawa utilizing an adhesive tape under the semiconductor element, since specific use of an adhesive tape is well known in the art and can provide a desired attachment between the semiconductor element and another surface.

Furthermore, examiner takes the position that the material selected for the adhesive layer under the semiconductor element, in view of those used in the prior art, is non-critical to the applicant's invention. Li and Nakazama discloses all the limitations of the claimed invention except for specifically teaching that "the adhesive is an adhesive tape." It would have been obvious to one of ordinary skill in the art, at the time of invention, to have the adhesive of Li and Nakazama's device to be one that is specifically made of an adhesive tape, since it has been held to be within the general skill of a person in the art to select a known material on the basis of its suitability for the intended use (to provide attachment for semiconductor element) as a matter of obvious design choice. *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

6. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US Patent No. 6,348,729) in view of Hashimoto (US Patent Application No. 10/244,162).

Li teaches, from figs. 6-10 and columns 3 and 4, a method of manufacturing a semiconductor device, comprising the steps of:

providing a flexible tape (250) having a plurality of terminals (222a, 224) in a product forming portion formed over a main surface of the tape, the terminals being formed by a metal film (see column 3, lines 16-26); (fig.6)

fixing a semiconductor element (210) to the main surface of the tape (250); (fig. 7)

connecting electrodes formed over the semiconductor element (210) and the terminals (222a, 224) with each other through conductive wires (230, 232); (fig. 8)

forming an insulating resin layer (240) in an area including the semiconductor element (210) and the wires (230, 232) over the main surface of the tape (250) to cover the semiconductor element (210) and the wires (230, 232); (fig. 9) and

peeling the tape (250) from the insulating resin layer (240) after covering the semiconductor element (210) and the wires (230, 232) with the insulating resin layer (240).

Li does not teach that wherein the tape is a band-like tape, and the fixing of the semiconductor element, the connection of the wires and the formation of the insulating resin layer are performed in this order in the longitudinal direction of the tape, and thereafter the tape is wound round a reel.

However, Hashimoto, drawn to the manufacture of semiconductor packages, teaches, from fig. 13, a carrier tape (10) (which has a plurality of terminals (14) on a plastic substrate (12)), after chip mounting (see paragraph [0122]) and resin covering (see paragraph [0091])

steps, that is wound around a reel (24 on left side of fig. 13) and undergoes reel to reel operations in a cutting stage.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the method of manufacture of Li whereby the tape is wound onto a reel as described by Hashimoto because reel to reel operation provides a smooth and continuous device fabrication (see paragraphs [0014] and [0107]) and, so long as the tape is flexible and can provide wiring, any tape can be used in this reel to reel operation. (See paragraph [0108])

7. Claims 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US Patent No. 6,348,729) in view of Fjelstad (US Patent No. 6,856,235).

With respect to claims 51 and 52, both containing similar subject matter, Li teaches, from figs. 6-10 and columns 3 and 4, a method of manufacturing a semiconductor device, comprising the steps of:

providing a flexible tape (250) having a plurality of terminals (222a, 224) in a product forming portion formed over a main surface of the tape, the terminals being formed by a metal film (see column 3, lines 16-26); (fig.6)

fixing a semiconductor element (210) to the main surface of the tape (250); (fig. 7)

connecting electrodes formed over the semiconductor element (210) and the terminals (222a, 224) with each other through conductive wires (230, 232); (fig. 8)

forming an insulating resin layer (240) in an area including the semiconductor element (210) and the wires (230, 232) over the main surface of the tape (250) to cover the semiconductor element (210) and the wires (230, 232); (fig. 9) and

peeling the tape (250) from the insulating resin layer (240) after covering the semiconductor element (210) and the wires (230, 232) with the insulating resin layer (240).

Li does not teach that a plurality of semiconductor elements is fixed to the product forming portion.

However, Fjelstad, drawn to the manufacture of resistors and chips using a sacrificial layer (see fig. 1A-1G), teaches, from fig. 4B, a plurality of semiconductor elements (170''' and 120''') in a product forming region (between electrodes 110''').

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the method of manufacture of Li utilizing multiple chips stacked on one another in a product forming region because stacking a plurality of chips is a very well known method for reducing the amount of circuit board area consumed by the integrated chip components and thereby can reduce the overall size of the board. (e.g. see Chen US Patent No. 6,365,966)

8. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US Patent No. 6,348,729) as applied to claim 53 above, and further in view of Hiramatsu (US Patent No. 6,609,297).

Li does not teach that an auxiliary metal layer having a rough surface is formed over the main surface of the main metal layer to provide a rough surface over the main surface side of each of the terminals.

However, Hiramatsu, drawn to printed wiring board design, teaches from fig. 4C, an auxiliary metal layer (23) having a rough surface is formed over the main surface of the main

metal layer (22A or 22B) to provide a rough surface over the main surface side of each of the terminals. (See column 11, lines 24-46.)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the method of manufacture of Li utilizing a rough electrode surface as described by Hiramatsu because this increases the adhesion strength between two layers joined at their surface due to the fact that a roughened surface increases the area of contact as opposed to a flat surface. Obviously, increased adhesion between layers lends itself towards a more durable and reliable product.

9. Claim 57 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US Patent No. 6,348,729) in view of Long (US Patent No. 5,173,766).

Li teaches, from figs. 6-10 and columns 3 and 4, a method of manufacturing a semiconductor device, comprising the steps of:

providing a flexible tape (250) having a plurality of terminals (222a, 224) in a product forming portion formed over a main surface of the tape, the terminals being formed by a metal film (see column 3, lines 16-26); (fig.6)

fixing a semiconductor element (210) to the main surface of the tape (250); (fig. 7)

connecting electrodes formed over the semiconductor element (210) and the terminals (222a, 224) with each other through conductive wires (230, 232); (fig. 8)

forming an insulating resin layer (240) in an area including the semiconductor element (210) and the wires (230, 232) over the main surface of the tape (250) to cover the semiconductor element (210) and the wires (230, 232); (fig. 9) and

peeling the tape (250) from the insulating resin layer (240) after covering the semiconductor element (210) and the wires (230, 232) with the insulating resin layer (240).

Li does not teach that of the steps of fixing the semiconductor element, connecting the wires and forming the insulating resin layer, one or plural steps are carried out while holding a back surface of the tape by vacuum suction.

However, Long, drawn to the manufacture of semiconductor packages, teaches, from figs. 6A and 6B, vacuum suction (through 610,a,b) is used to hold the back surface of the tape (551) in the step of fixing a semiconductor element (24) to a carrier tape assembly (551). Also, vacuum suction (through hole 710b) used during wire connection process. (See fig. 7a and column 26, lines 34-37.)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the method of chip manufacturing of Li utilizing a vacuum suction process - as described by Long - to hold the tape in place during chip placement, wiring connection, and resin molding steps because this process provides a stable and accurate environment for these steps to be carried out (see column 26, lines 44-46) and the fact that vacuum holding is well known in the art. (See column 3, lines 28-32)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Kunzer whose telephone number is (571) 272-5054. The examiner can normally be reached on Monday-Friday 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
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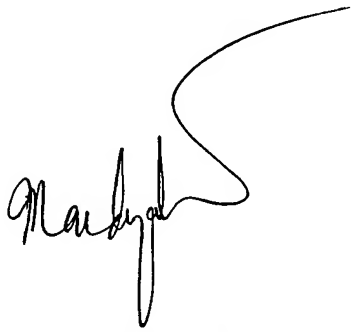

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